WHAT IS CLAIMED IS:

1. A data selection circuit for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the data selection circuit being connected to receive the debug data and comprising:

logic for receiving the debug data as a plurality of *N*-bit portions of block-aligned data and outputting a designated one of the *N*-bit portions; and

circuitry for providing to the receiving logic a control signal for designating one of the *N*-bit portions.

2. The data selection circuit of claim 1 wherein the logic for receiving comprises a multiplexer (MUX) circuit including a plurality of sets of inputs and one set of outputs, wherein each of the *N*-bit portions is input to a respective one of the sets of inputs.

3. The data selection circuit of claim 2 wherein the control signal is input to the MUX circuit for selecting one of the sets of inputs to be output via the set of outputs.

4. The data selection circuit of claim 2 wherein the MUX circuit comprises 16 eight-input MUXes.

5. The data selection circuit of claim 1 wherein the circuitry for providing the control signal comprises a control status register ("CSR").

6. The data selection circuit of claim 1 wherein the debug data comprises 80 bits.

7. The data selection circuit of claim 1 wherein *N* is equal to 16.

8. The data selection circuit of claim 1 wherein the debug data comprises eight 10-bit-block-aligned portions.

9. A data selection circuit for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the data selection circuit being connected to receive the debug data and comprising:

means for receiving the debug data as a plurality of *N*-bit portions of block-aligned data and outputting a designated one of the *N*-bit portions; and

means for designating to the receiving means one of the *N*-bit portions.

10. The data selection circuit of claim 9 wherein the receiving means comprises a multiplexer (MUX) circuit including a plurality of sets of inputs and one set of outputs, wherein each of the *N*-bit portions is input to a respective one of the sets of inputs.

11. The data selection circuit of claim 10 wherein the designating means comprises a control signal input to the MUX circuit for selecting one of the sets of inputs to be output via the set of outputs.

12. The data selection circuit of claim 10 wherein the MUX circuit comprises 16 eight-input MUXes and wherein each of the eight-input MUXes receives one bit of each of the *N*-bit portions.

13. The data selection circuit of claim 9 designating means comprises a control status register ("CSR") containing a select signal.

14. The data selection circuit of claim 9 wherein the debug data comprises 80 bits.

15. The data selection circuit of claim 9 wherein *N* is equal to 16.

16. The data selection circuit of claim 9 wherein the debug data comprises eight 10-bit-block-aligned portions.

17. A method of implementing data selection for a general purpose performance counter ("GPPC") connected to a bus carrying debug data, the method comprising:

receiving the debug data as a plurality of *N*-bit portions of block-aligned data; and

outputting a designated one of the *N*-bit portions based on a selection control signal.

18. The method of claim 17 wherein the selection control signal is provided by a control status register (CSR).

19. The method of claim 17 wherein the operation of outputting a designated one of the N-bit portions further comprises:

inputting each of the *N*-bit portions to a corresponding set of data inputs of a MUX circuit;

providing the selection control signal to the MUX circuit for selecting one of the sets of inputs; and

outputting via a set of outputs data input to the selected set of inputs.

20. The method of claim 17 wherein the debug data comprises 80 bits.

21. The method of claim 17 wherein *N* is equal to 16.

22. The method of claim 17 wherein the debug data comprises eight 10-bit-block-aligned portions.